

## **ABSTRACT OF THE DISCLOSURE**

A line predictor caches alignment information for instructions. In response to  
5 each fetch address, the line predictor provides alignment information for the instruction  
beginning at the fetch address, as well as one or more additional instructions subsequent  
to that instruction. The alignment information may be, for example, instruction pointers,  
each of which directly locates a corresponding instruction within a plurality of instruction  
bytes fetched in response to the fetch address. The line predictor may include a memory  
10 having multiple entries, each entry storing up to a predefined maximum number of  
instruction pointers and a fetch address corresponding to the instruction identified by a  
first one of the instruction pointers. Fetch addresses may be searched against the fetch  
addresses stored in the multiple entries, and if a match is detected the corresponding  
instruction pointers may be used. Additionally, each entry may include a link to another  
15 entry storing instruction pointers to the next instructions within the predicted instruction  
stream. Furthermore, the entries may store a next fetch address corresponding to the first  
instruction within the next entry. The next fetch address may be provided to the  
instruction cache to fetch the corresponding instruction bytes. Still further, additional  
control information corresponding to the identified instructions may be included.

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